

## REMARKS

These comments are responsive to the dated August 22, 2006, for which a one-month extension is hereby requested. Non-elected claims 18-27 and 43 are being cancelled. In response objection to the Specification, paragraph [0080] has been amended as indicated above. In response to the rejection of claim 14, under 35 U.S.C. § 112, second paragraph, claim 14 has had its dependence changed and now has the appropriate antecedent basis for the claim elements. The Office Action rejected pending claims 1-17 and 28-42 under either 35 U.S.C. § 102(b) as being anticipated by Estakhri et al. (US Patent No. 5,835,935) or under 35 U.S.C. § 103(a) with Estakhri as the primary reference. It is respectfully submitted that these prior art rejections are in error.

### Claims 28-42

Claims 29-42 are all dependent claims having claim 28 as their base claim. Claim 28 is rejected under 35 U.S.C. § 102(b) as being anticipated by Estakhri et al. (US Patent No. 5,835,935). Claim 28 relates to an aspect of the present application whereby the controller accesses the memory by a set of metablock linkings that the controller establishes in a deterministic way:

A memory system including a controller and a non-volatile memory, wherein the non-volatile memory is comprised of a plurality of units of erase, wherein the controller accesses the non-volatile memory according to a set of *metablock linkings*, each comprised of a plurality of units of erase, wherein the controller establishes the set of metablock linkings in a deterministic manner.

As the emphasis, which is added, highlights, these linkings are for metablocks. Metablocks (also known as "super" blocks) are discussed in the application generally in paragraphs [0008] and [0009], with various aspects of these structures presented throughout the application.

In a flash type memory, the physical unit of memory by which the memory is erased is a block, typically composed of one or more sectors. A metablock is a logical unit in which *multiple logical* blocks are combined into a composite entity that the controller addresses as a single logical unit, which the logical-to-physical conversion then maps to a corresponding number of physical blocks, allowing multiple physical blocks to be accessed for erase or program in parallel as a single logical unit.

In the cited locations, the Estakhri references also present a linking, but of a very different nature where *multiple physical* units of the memory are linked to only a *single* VIA EFS

corresponding *logical* unit. This difference can be explained by referring to Estakhri's Figures 3 and 4 and the corresponding description in lines 32-53 of column 4. As shown in these figures, the memory in Estakhri (or, rather, a part of the memory) is organized multi-sector clusters. As shown in Figure 4, each of these clusters is a single physical block having physical block address (PBA) and which is assigned a logical block address (LBA). Only one sector in a given cluster is current ("used") at any given time, with the preceding sectors of the cluster being "old" (having been superseded by the current "used" sector) sectors and the subsequent sectors being "free" for future use as the sector is updated. All of these elements of a given cluster are addressed by the same single logical address. As shown in Figure 4, once a given cluster fills up a given physical block (such as that with PBA 2), the process can continue on in another physical block (PBA (N+1) in the example), but the *same logical* address (LBA 2) is used for both physical blocks (PBA (N+1) and PBA 2). So although multiple physical blocks may be linked, only one has the current (non-"old") data, and they all correspond to the same logical address. There is no combining of *multiple logical* blocks into a composite unit (or metablock).

So under the arrangement of Estakhri, a single logical block address (LBA) is associated with one or more physical block addresses in a one to many mapping of logical addresses to physical addresses. These linkings do not form *metablocks* as the term is understood in the art or, in any case, as this is defined in the present application. In contrast, for a metablock linking, for some integer  $i > 1$ ,  $i$  LBAs are linked into a composite unit that is written into  $i$  PBAs according to a logical-to-physical mapping. This difference between a metablock linking and the linking of Estakhri can be illustrated by referring again to Estakhri's Figures 3 and 4: what Estakhri describes is what could be called, roughly, a "vertical" linking where one or more physical blocks are linked in a "temporal" direction as sectors are updated with new information, but which always correspond to a single logical block; in contrast, a metablock linking is, conceptually, a horizontal linking of *multiple* logical blocks that is maintained as the data is written or updated into a corresponding number of physical blocks. Estakhri neither teaches nor suggests a metablock linking where multiple logical block addresses are formed into a composite logical structure.

Consequently, for at least these reasons, it respectfully submitted that a rejection of claim 28 along with its dependent claims 29-42 under either 35 U.S.C. § 102(b) as being anticipated by Estakhri or under 35 U.S.C. § 103(a) with Estakhri as the primary reference is in error and

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should be withdrawn. Although it is believed that a number of these dependent claims are further allowable for the additional limitations they recite, as the independent claim is already believed to be quite distinct from what the Office Action is presenting from the prior art, these additional reasons will not be given at this time.

#### Claims 1-17

Claims 2-17 are all dependent claims having claim 1 as their base claim. Claims 1-17 are all rejected under 35 U.S.C. § 103(a) as unpatentable over Estakhri et al. (US Patent No. 5,835,935) in view of Chien et al. (US Patent No. 6,742,078). Claim 1 relates to an aspect of the present application whereby the controller the accesses the memory by a set of metablock linkings that the is established and stored in the non-volatile memory:

A method of operating a memory system including a controller and a non-volatile memory, wherein the non-volatile memory is comprised of a plurality of units of erase, the method comprising:

establishing a set of *metablock linkings*, each comprised of a plurality of units of erase, by which the controller accesses the non-volatile memory; and  
storing a record of said *metablock linkings* in the non-volatile memory.

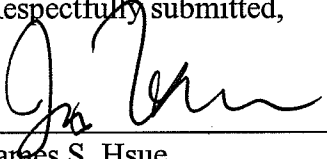
As the emphasis, which is added, highlights, these linking are for metablocks, as discussed above with respect to claim 28. The Estakhri reference is again cited for “establishing a set of *metablock linkings* ...”; as discussed with respect to claim 28, although the Estakhri reference does use a linking of sorts, this is not a metablock linking. For the step of “storing a record of said *metablock linkings* ...”, the Office Action cites Chien which presents a “link-table”; however, this “link-table” is also not for metablock linking, but for the logical-to-physical conversion of (single) block addresses. Consequently, neither Estakhri nor Chien, whether alone or in conjunction, teach or suggest the sort of metablock linking found in claim 1.

Consequently, for at least these reasons, it respectfully submitted that a rejection of claim 1 along with its dependent claims 2-17 under 35 U.S.C. § 103(a) as unpatentable over Estakhri in view of Chien is in error and should be withdrawn. Although it is believed that a number of these dependent claims are further allowable for the additional limitations they recite, as the independent claim is already believed to be quite distinct from what the Office Action is presenting from the prior art, these additional reasons will not be given at this time.

Conclusion

For the reasons above, it is believed that the various rejections of claims 1-17 and 28-42 are not well founded and should be withdrawn. Reconsideration of these claims and an early indication of their allowability and an early indication of their allowance are earnestly solicited.

Respectfully submitted,

  
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12/13/06  
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